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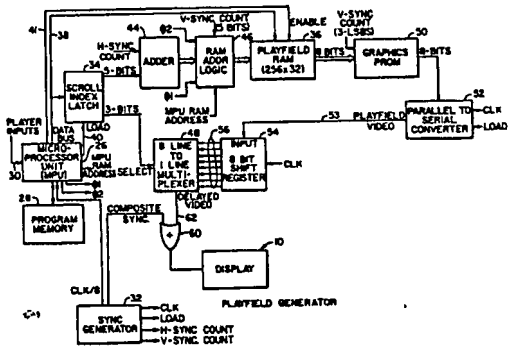
(54) Apparatus for scrolling a video display.

(57) Apparatus for displaying symbols, e.g. in a video game, is operable to scroll playfield objects appearing on the display unit (10) of the game by selectively altering the address used to access an addressable random access memory (36) containing data indicative of the objects displayed. The address is altered in accordance with a portion of an index in a temporary store (34). The random access data, when accessed, is used to address a video data memory (50) which provides pictorial video data for the video display. Further scrolling effect can be obtained by selectively delaying the video data communicated to the video display unit (10) in response to a further portion of the intex.



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APPARATUS FOR SCROLLING A VIDEO DISPLAY

Background of the Invention

The present invention is directed to apparatus for generating signals for displaying symbols on a video raster-type display and particularly,but not exclusively, to a video game in which the display is scrolled in the horizontal direction under synchronous microprocessor control in response to player inputs.

In a video system where it is desired to display selected video portions of a larger available field, one technique has been to use a mechanical pictorial map with the television camera on an XY table; that is, a table which moves left and right or up and down. Such a technique is termed "scrolling" since the field is effectively being scrolled past the video camera from a relative motion standpoint. An analogous nonmechanical known technique uses a large capacity graphics computer which has the entire field stored in a pictorial memory, the computer providing a window on that memory to produce the display world on the TV screen. This latter method, of course, requires a very large program memory.

One technique for scrolling in the vertical direction only is shown in U.S. Patent No. 4,169,272, issued 25th September 1979, entitled "Apparatus for Simulating a Perspective View of a Video Image and for storing Such Image with a Minimum Number of Bits" in the name of Rains, et al. This technique utilizes a vertical counter to directly address a graphics read-only memory (ROM) at different locations. Such a ROM, of course, includes the entire field. The technique, however, is not particularly adaptable to scrolling in a horizontal direction.

It can be seen, therefore, that there exists a need for apparatus capable of scrolling a video display in a horizontal direction, which utilizes a minimum of memory space and circuitry. Such a technique would obviate the need

for expensive and complex apparatus such as television cameras or large program memories described above.

Summary of the Invention

This invention provides apparatus for generating signals for displaying symbols on a video raster-type display, the apparatus comprising memory means for storing data representative of the symbols, and address means for addressing said memory means in order to cause said signals to be provided in response to said data, the apparatus being operable to cause scrolling of the displayed symbols, characterised in that said memory means comprises:

first memory means for storing at addresses corresponding to locations on the video display, data indicative of the display symbols; and

second memory means for containing pictorial video data representative of said symbols, the second memory means being responsive to the data of the first memory means to provide said signals;

said address means being operable to communicate an address to said first memory means to cause the data at that address to select corresponding pictorial video data in said second address means;

and further characterised in that said address means includes means for temporarily storing an index, said address means being responsive to said index for generating the address to be communicated to said first memory means, whereby the display location to which addresses correspond can be altered, and said scrolling thereby achieved, by altering said index.

Brief Description of the Drawings

Figs. 1A-1C are plan views of video images illustrating the present invention;

Fig. 2 is a conceptual illustration of an entire playfield capable of being displayed and showing the portion of the field selected for display;

Figs. 3A-3B are examples of the building block graphics used to construct a playfield display;

Fig. 4 is a map of the information stored in the RAM and illustrates the correlation between the RAM information and the building block graphics stored in a graphics PROM;

Fig. 5 is a block diagram illustrating the circuit logic used to practice the method of the present invention;

Fig. 6 is a representative timing diagram illustrating access to the RAM on a time-share basis; and

Fig. 7 is a diagrammatic illustration of a portion of the contents of the RAM.

Detailed Description of the Preferred Embodiments

The present invention is most advantageously practiced in conjunction with generating objects on a video display screen of the type utilizing an image-forming beam that traverses the screen along a plurality of sequentially scanned horizontal lines. Movement of the beam is synchronized to the video data supplied by the invention by conventional horizontal and vertical synchronizing signals, including horizontal and vertical retrace intervals.

Typical video images and the sequential relationship between them, as they are shown on video display screen 10, are illustrated in Figs. 1A-1C and 2, the Figures 1A-1C being shown in relative progressing time sequences. These video images are used in a game termed "FOOTBALL" where game players, by means of manually

controllable input devices, control the relative position of the movable objects displayed in accordance with certain instructions that are provided. For the purpose of the following discussion, it should be understood that the video scan lines generated on display 10 by the image-forming beam are oriented perpendicular to the yard lines designated in Figs. 1A-1C by the reference numeral 12.

Typically, video objects displayed on video display screen 10 may be categorized as playfield objects and movable objects. Playfield objects, such as yard lines 12, the numerals 14, and direction pointers 15, are termed playfield objects which are scrolled as an indirect result of player inputs. The second category, termed movable objects, comprise offense players designated by O's 16, including ball carrier 18, and defense players designated by X's 20.

Conceptually, the playfield objects shown on video display screen 10 are a selected portion of a larger field of playfield objects; that is, as Fig. 2 illustrates, display 10 presents a viewer with a window-like view A of a larger field B. Here, the view A is movable along the field B between the opposing representative goal lines G. The field B may be thought of as being broken up into an M by N matrix of smaller building blocks - termed "stamps" - for the purpose of displaying these various playfield building blocks or stamps to construct the actual video display elements making up the field (e.g., yard markers 12 and numerals 14) as well as other information such as messages (not shown). As described more particularly below, these stamps are listed and have their actual video display characteristic or shape stored in a graphics memory. A yard line 12, for example, is composed of several stamps which are selected and arranged in proper format for display as will be more

particularly discussed. As Fig. 1B indicates, the video produced on display 10 is formed from a 30 x 30 array of these stamps.

The game is played by players selecting offensive and defensive plays to set the game in motion. Operation of manual controls by players of the game will effect movement of objects 16, 18 and 20. Thus, for example, a player operating controls (not shown) that effect and direct movement of the "offensive" movable objects 16 and 18 can cause them to move away from the representative 30-yard line and toward the 40-yard line (Fig. 1A). At the same time, of course, the defensive player would manipulate controls to move the defense movable objects 20 in an attempt to establish video display coincidence between at least one of the defensive movable objects 20 and ball carrier 18 to establish a representative tackle. Depending upon the success (or lack thereof) of the game players in controlling their respective ones of the movable objects 16, 18 or 20, representative movement of the field of play between goal lines G will be effected by sequentially displaying selected portions of the overall field B, i.e., by "scrolling" the field B. Thus, for example, one play of the game may commence at a field position as represented by Fig. 1A and progress as illustrated by Fig. 1B and then by Fig. 1C.

As the ball carrier object 18 moves in either direction between goals G of the representative field, the yard line markers and numerals associated therewith move in a direction (a horizontal direction as viewed in Figs. 1A-1C) that simulates travel of the motion objects along the length of the field B.

The present description concerns only the generation of playfield objects. Movable object generation can be accomplished in the manner disclosed in U.S.

Patent No. 4,116,444, but is preferably accomplished in accordance with the teachings of our co-pending European patent application No. 79302396.1. The disclosure of each of the above is hereby incorporated by reference.

The field B exists only in theory, and selected portions of the information required for specifying the graphics to be displayed are periodically constructed and stored in a random access memory (RAM) by a microprocessor unit as will be described below. For the purposes of the present discussion, however, it is convenient to think of the field B as existing in some memory location as an ordered matrix of stamp selection information.

There are, in fact, relatively few stamps used to construct a playfield display. Figs. 3A and 3B illustrate two representative stamps. Fig. 3A illustrates the stamp of a yard marker segment 12a, while Fig. 3B illustrates an alpha numeric stamp comprising a zero numeral 14a, pointer 15 and a yard marker segment 12a. Other stamps used in the football game under discussion include the numerics 1-5, and the letter G to designate the goal line. As will now be apparent, yard marker stamps, such as that shown in Fig. 3A, are displayed in a vertical column to form one of the yard markers 12 illustrated in Figs. 1 and 2.

In the preferred embodiment, each stamp is an 8 x 8 element array of data bits used to form the actual display graphics. Elements in both the horizontal and vertical directions are the smallest resolution elements of the video display which has, as indicated in Fig. 1A, 240 elements (beam positions) for each horizontal line and 240 raster lines. Thus, a playfield is constructed on display 10 by selecting and positioning the desired stamps to form a 30 x 30 stamp array on the display (Fig. 1B).

The information indicative of the relative position of each stamp to be displayed is stored in a random access memory. This information is used to address a graphics programmable read-only memory (PROM) in which the stamps are stored, the output of which provides the actual graphics for the video display. The information stored in the RAM is arranged so that sequential addressing of the RAM will cause the PROM to provide the graphics necessary for an ordered 30 x 30 array of stamps. Thus, data stored in the RAM is only indicative of the video display.

Fig. 4 illustrates the correlation between the contents of the RAM and PROM. As indicated, the RAM has 32 x 32 storage locations, each storage location being one byte (eight digital bits) in size. During actual scan time (i.e., during display of one video field of playfield graphics) only the graphics specified by the information stored in the 30 x 30 RAM portion designated by reference numeral 21 is actually displayed. However, the entire RAM portion designated by reference numerals 21, 22 and 22' is addressed. The information stored in the one-byte columns 22 and 22' are used for updating purposes described below and do not result in the display of graphics in video display 10. A row 23 of stored information is used for control of the movable objects 16, 18, 20, which forms no part of this invention.

As noted above, each of the addressable entries of memory portion 21 of the RAM is permanently associated with or corresponds to a unique location in the video display 10. The information kept at each RAM entry designates the particular location in the PROM containing the stamp to be displayed at the video display location corresponding to that entry. For example, as Fig. 4 illustrates, entry 21a contains information that, when applied to the PROM, causes the PROM to provide stamp 24.

The next sequential entry 21b causes the PROM to provide stamp 25.

As Fig. 4 also illustrates, each stamp comprises 8 bytes, each byte containing 8 bits of graphics data, used when assembled to form the 8 x 8 stamp array referred to above. Further, each of the RAM entries designates an 8-byte stamp - just as, for example, entry 21a designates the 8 bytes 24a-24h that comprise stamp 24 in Fig. 4. Similarly, the next successive RAM location 21b designates stamp 25 comprising 8 bytes 25a-25h. Selection of the individual ones of the bytes 24a-24h and 25a-25h to be displayed during each horizontal line scan is accomplished in the manner described below.

Turning now to Fig. 5, the playfield generator of the present invention includes a microprocessor 26 to which is connected a program memory 28 to provide for overall control of the various units comprising the apparatus. Input ports 30 to the microprocessor 26 communicate motion signals from the player controls (not shown) to the microprocessor 26. Timing pulses for synchronizing microprocessor control with the display video, as well as for providing control for various playfield generator functions, are generated by a sync generator 32. Thus, sync generator 32 provides a first clock (CLK) signal used by the generator to effect certain synchronous clocking operations and a second clock (CLK/8) signal for use by microprocessor 26. In addition, the sync generator 32 contains internal horizontal and vertical sync counters (not shown) clocked by the CLK signal and which produce H-sync and V-sync counts, respectively. Each counter is a modulo 256 counter and the counts produced are used for control and addressing functions of the playfield generator as will be described. These counts (i.e., H-sync and V-sync) are also used by sync generator 32 to produce a composite sync signal which is

combined with the video generated by the playfield generator to drive display 10. In effect, therefore, the H-sync and V-sync counts provide the playfield generator with information specifying the position of the beam used to construct display 10 during each line scan. Finally, sync generator 32 provides a periodic load signal (LOAD) to effect information transfers, as will be explained below.

Microprocessor 26 is coupled to a scroll index latch 34 and a playfield random access memory (RAM) 36 by a data buss 38, which communicates digital information to these elements - typically in one-byte (eight bit) segments. Microprocessor 26 is also coupled to the scroll index latch 34 by a load line 40 which commands the latch to accept and temporarily store information appearing upon the data buss 38. Similarly, an enable line 41 communicates write instructions from the microprocessor to the playfield RAM 36 to cause the RAM to store data present on the data buss 38.

The scroll index latch 34 stores one-byte (eight bits) of digital information. A first portion of each byte (five of the eight bits in the preferred embodiment) of information held by the scroll index latch 34 is communicated to playfield RAM 36 via an adder 44 and a RAM address logic unit 46. A second portion of the same byte (the three remaining bits) held by scroll index latch 34 is communicated to an 8-to-1 multiplexer 48.

The RAM 36 is capable of being addressed by the microprocessor 26 or by adder 44 and a portion of V-sync count in direct memory access (DMA) mode. In order to address the 32 x 30 array (equalling 960 bytes) of stamp positional information formed by RAM portions 21, 22 and 22' (Fig. 4), at least a 10-bit address is required, which provides the capability of addressing 2^{10} or 1024 locations. The address generated for RAM access during

DMA mode (hereinafter designated the DMA generated address) comprises the five most significant bits (MSB's) of V-sync count (which selects one of 30 lines of 32 bytes), and a five-bit sum of the five MSB's of H-sync count and the first (5-bit) sum of the five MSB's of H-sync count and the first (5-bit) portion of the scroll index (which selects one of the 32 byts in the selected line). Any carry generated is discarded.

It should be noted that the DMA generated address provides, in effect, modulo 32 addressing of the 32 bytes in each row of the 32 x 30 byte playfield array stored in RAM 36. That is, the five MSB's of H-sync count provide the addressing for 32 bytes during each horizontal scan time. However, by adding the 5-bit portion of the scroll index to H-sync count, a row of 32 bytes is still addressed, but the first and each succeeding byte read out of the RAM 36 are shifted in time or offset by the 5-bit portion of the scroll index - relative to H-sync count.

Fig. 7 is a schematic illustration of this offset. Portions 21, 22 and 22' of the RAM map of Fig. 4 are shown as a cylinder with the left and right edges of the map joined at vertical line C. If the 5-bit portion of the scroll index (contained in scroll index latch 34) is zero, no offset is effected. The DMA generated address begins at row V1, byte B1 and sequentially addresses each succeeding byte of the row V1 until byte B32 is reached, at which time addressing begins again with byte B1 of either row V1 or the next succeeding row V2. If, however, the 5-bit portion of the scroll index is non-zero, the H-sync count is offset by a corresponding amount, and addressing begins and ends with different bytes in the same row. Thus, for example, if the 5-bit portion of the scroll index increases or offsets H-sync count by one, the addressing of each row (V1-V30) of the

map begins at byte B2, progresses through to B32 and ends by addressing byte B1; that is, the RAM map 70 has been precessed by one byte from vertical line C to vertical line D. The effect is to scroll the video display by one stamp column.

The RAM address logic 46 contains logic circuitry of known design that selects the addressing (MPU RAM addressing or the DMA generated address) for RAM 36 in several ways. First, the RAM address logic 46 communicates the MPU RAM address from the microprocessor 26 to the RAM during the horizontal and vertical retrace intervals. During active scan time, the address logic 46 interleaves communication of an address formed by the information provided by adder 44 and V-sync count with the MPU RAM address to the RAM. This interleaving is accomplished in response to Ø1 and Ø2 clock signals provided by microprocessor 26. The relationships between the Ø1, Ø2 and CLK signals are illustrated in Fig. 6; Ø1 and Ø2 are generated by the microprocessor from the CLK/8 signal provided by the sync generator 32. The Ø1 and Ø2 clock signals (as is the CLK/8 signal) are the CLK signal divided by eight.

The RAM 36 address interleaving is accomplished by multiplexing the MPU RAM address and the DMA generated address using the Ø1 and Ø2 signals as a multiplex control. Thus, during the time designated as T1 in Fig. 6, the DMA generated address is gated to the RAM 36; during the time designated as T2, the MPU RAM address is gated to the RAM 36.

As noted above, playfield RAM 36 contains data at specific addressable locations that are indicative of the display position of the various playfield building block stamps. These stamps are listed and have their actual display characteristics or shape stored in a graphics PROM 50. Graphics PROM 50 is controlled by

playfield RAM 36, in conjunction with the three least significant bits (LSBs) of V-sync count to access the actual video display from the PROM in eight-bit segments. The manner of access establishes the arrangement and appropriate format in which the video data is to be presented on the display screen to form the particular view A of the conceptual overall field B, as indicated in Figs. 1 and 2.

The graphics information provided by the PROM 50 is obtained by applying to the PROM an address formed from the combination of one byte of information from the RAM 36 and the three LSBs of V-sync count. The RAM information selects the particular stamp and the three LSBs of V-sync count select the particular 8-bit byte of the stamp. Thus, each one of the 30 lines of 32 bytes (Fig. 4) is read out of the RAM 36 eight consecutive times, during each field of display.

The eight bits of information provided by graphics PROM 50 are communicated and applied to parallel inputs of parallel-to-serial converter 52. The information is accepted by the converter upon receipt of the LOAD signal from the sync generator 32. Then, in response to the CLK signal, the contents of converter 50 are shifted out of the converter onto line 53, forming serial playfield video. This playfield video is applied to the input of an eight-stage, serial shift register 54, also clocked by the CLK signal. The eight parallel outputs 56 (one output from each stage) of the shift register 54 are applied to the multiplexer 48. The multiplexer 48 selects one of the eight parallel shift register outputs 56 and communicates the selected output to a summer 60 via delayed video line 62, where it is combined with composite sync from generator 32 to drive display 10.

The video display graphics information applied to the serial input of the shift register 54 is shifted through the various eight stages (not shown) of the register in response to the CLK signal applied thereto. Depending upon the states of the three bits applied to the multiplexer 48 from the scroll index latch 34, one of the eight outputs 56 of the shift register 54 is selected for communication to the video line 62 via the multiplexer 48. The playfield video displayed during the active television line is thus delayed, and therefore relatively positioned along the line, as a result of which one of the eight shift register outputs 56 is communicated to summer 60.

The playfield RAM 36 is updated as often as every third vertical blanking interval. That is, in the time period between each update of the playfield RAM, the scrolling of view A along field B (Fig. 2) has not effectively advanced far enough to necessitate an updating of the RAM. This is due in part to the fact that some scrolling of the video display is effected to some extent by delaying the video applied to the summer circuit 60. However, when the playfield RAM is updated, only one of the two columns 22, 22' of information is loaded - corresponding to the (left or right) edge of the display 10 toward which motion is proceeding.

In operation, microprocessor 26 receives player information on input ports 30 and computes playfield stamp selection information that is stored in RAM 36. During display time the RAM 36 and the PROM 50 are sequentially addressed by the H-sync and V-sync counts generated by sync generator 32. As the game progresses, requiring the playfield to be scrolled, a scroll index is calculated with the three-bit portion modified from that presently held by scroll index 34. During the next vertical blanking interval, the newly calculated scroll

index is transferred to and stored in the scroll index latch 34 by the microprocessor 26. The new three-bit portion of the scroll index effects selection of a new one of the eight parallel shift register outputs 56 to cause the graphics information of each active horizontal scan line appearing on the video display to be delayed, depending upon which of the outputs 56 is selected. The video display is thus scrolled.

However, scrolling by video delay is effective for seven horizontal bits only. Once the maximum video delay is selected, the RAM 36 must be updated with a new column of information for selecting a new (vertical) column of stamps to be displayed. In addition, the 5-bit portion of the scroll index must be updated so that the H-sync count portion of the DMA generated address is offset by one to precess the addressing of RAM 36 as explained above. The 3-bit portion is also updated as appropriate. This update of RAM 36 and scroll index latch 34 can be done during the same or different vertical blanking period, so long as the RAM 36 is updated first.

In summary, the present invention effects scrolling in the scan line axis in two respects: First, the video display is scrolled by a video delay technique; this technique provides a scrolling effect having a minimum resolution equal to one horizontal bit (i.e., beam position along a given scan line) and a maximum range of seven bits. Second, a scrolling effect is produced by updating the RAM 36 with one column (30 bytes) of stamp selection information of 30 stamps and then offsetting the address applied to the RAM 36 so that the RAM is accessed at a shifted location. As noted above, 32 stamp elements are accessed from PROM 50 during each of the 240 (8 x 30) horizontal scan lines. However, the horizontal blanking of video display 10 is set so

that the two stamp elements in columns 22 and 22' are blanked each scan line; thus, only 30 stamp elements are displayed during each active scan line of video display 10. Because new information is written into the RAM 36, scrolling can be performed over as large a range as is desired.

As will now be apparent, the present embodiment provides apparatus for scrolling a video display presented in raster-type format in a direction along the display lines with a minimum of additional circuitry. More specifically, the amount of memory storage required to completely define the game playfield elements (i.e., the size of the graphics PROM 50) is minimized. Thus, for games having a relatively simple playfield, such as football, a PROM of only minimal size is required. Alternatively, a plurality of sets of stamps, each defining a different playfield, may be stored in a single PROM of reasonable size, thus permitting the construction of a video game apparatus affording a wide variety of different games, with some or all of the games having the scrolling feature.

While the above provides a full and complete disclosure of the preferred embodiment of the present invention, various modifications, alternate constructions and equivalents may be employed without departing from the true spirit and scope of the invention. For example, some scrolling can also be effected in the vertical direction by offsetting the V-sync count used to address the RAM 36 as well as by updating the RAM with lines of information of 32 stamps. Therefore, the above description and illustrations should not be construed as limiting the scope of the invention, which is defined by the appended claims.

CLAIMS:

1. Apparatus for generating signals for displaying symbols on a video raster-type display (10), the apparatus comprising memory means (36,50) for storing data representative of the symbols, and address means (34,44, 46) for addressing said memory means in order to cause said signals to be provided in response to said data, the apparatus being operable to cause scrolling of the displayed symbols, characterised in that said memory means comprises:

first memory means (36) for storing at addresses corresponding to locations on the video display (10), data indicative of the display symbols; and

second memory means (50) for containing pictorial video data representative of said symbols, the second memory means (50) being responsive to the data of the first memory means (36) to provide said signals;

said address means (34,44,46) being operable to communicate an address to said first memory means (36) to cause the data at that address to select corresponding pictorial video data in said second memory means (50);

and further characterised in that said address means (34,44,46) includes means (34) for temporarily storing an index, said address means being responsive to said index for generating the address to be communicated to said first memory means (36), whereby the display location to which addresses correspond can be altered, and said scrolling thereby achieved, by altering said index.

2. Apparatus as claimed in claim 1, further characterised by means (48,54) responsive to a portion of said index for selectively delaying said output signals.

3. Apparatus as claimed in claim 2, characterised in that the delaying means includes shift register means (54), having an input (53) and a number of outputs (56), and means (48) responsive to said portion of said index for selectively communicating a one of the shift register means outputs (56) to said display (10).

4. Apparatus as claimed in any preceding claim, including means (32) for generating horizontal and vertical timing signals, and horizontal and vertical counter means for counting the respective timing signals, characterised in that said horizontal and vertical counter means is coupled to said address means (34,44,46), said address means including means (44,46) for combining a portion of said index with horizontal and vertical counts from said counter means to form said address communicated to the first memory means (36).

5. Apparatus as claimed in claim 4, characterised in that said vertical counting means communicates with said second memory means (50), the vertical count from said vertical counting means causing predetermined portions of the pictorial video data to be selected.

6. Apparatus as claimed in any preceding claim, characterised in that the second memory means is a programmable read-only memory (50).

7. Apparatus as claimed in any preceding claim, characterised by microprocessor means (26) coupled to the address means (34,44,46) and the first memory means (36) for providing said data indicative of the display symbols; means (32) for generating a clock signal having at least a first and a second state, the clock means (32) being coupled to said address means (34,44,46); and the address means including means (46) for communicating the address means to said first memory means (36) during the first state and for communicating said microprocessor means (26) to said first memory means (36) during the second state.

8. An apparatus for scrolling display symbols on a video raster-type display screen of the type having image-forming means including a controllable electron beam forming a plurality of horizontal lines upon the display screen in response to horizontal and vertical timing signals, the apparatus comprising:

horizontal and vertical counter means (32) responsive to the horizontal and vertical timing signals for generating counter output signals indicative of the position of the electron beam relative to the display screen;

memory means (36,50) for storing data representative of the display symbols;

addressing means (44,46) coupled to the memory means (36,50) and responsive to the counter output signals for generating a plurality of addresses to be applied to the memory means (36,50) for accessing said data to provide the video data signals corresponding to said display symbols; and

means (52,53,54,56,48,62,60) for communicating said video data signals to the display (10);

characterised in that said memory means comprises first memory means (36), addressable by said addressing means (44,46), for storing data indicative of the display symbols at addresses corresponding to locations on the video display (10), and

second memory means (50) for storing video data representative of a plurality of different objects, said objects forming the display symbols appearing on the video display (10), the second memory means (50) being responsive to the data of the first memory means (36) for providing said video data signals;

and further characterised in that means (26,34) are coupled to said addressing means (44,46) for generating an index word;

the addressing means (44,46) being operable to combine at least a first portion of the index word with said counter output signals to modify said addresses generated so as to scroll the display symbols; and

means (48,54) being provided responsive to a second portion of the index for selectively delaying communication of the video data signals to the video display (10), also to scroll said display symbols.

9. Apparatus as claimed in claim 8, characterised in that index generating means includes a microprocessor means (26).

10. Apparatus as claimed in claim 8 or 9, characterised in that the delay means includes serial shift register means (54) having an input (53) for receiving the video data signals provided by the second memory means (50) and a number of outputs (56), the delay means further including means (48) for selecting a one of the number of outputs (56) and for communicating said selected output to the video display (10).

11. Apparatus as claimed in any preceding claim characterised by means (26) for entering new data, indicative of symbols which are to be brought into view by a scrolling operation, into said first memory means (36) at addresses which, after alteration of said index to effect said scrolling operation, correspond to display locations at an edge of the display towards which the scrolling takes place.

12. Apparatus as claimed in any preceding claim characterised in that the apparatus is arranged to cause scrolling in the direction of the display lines of the raster-type display (10).

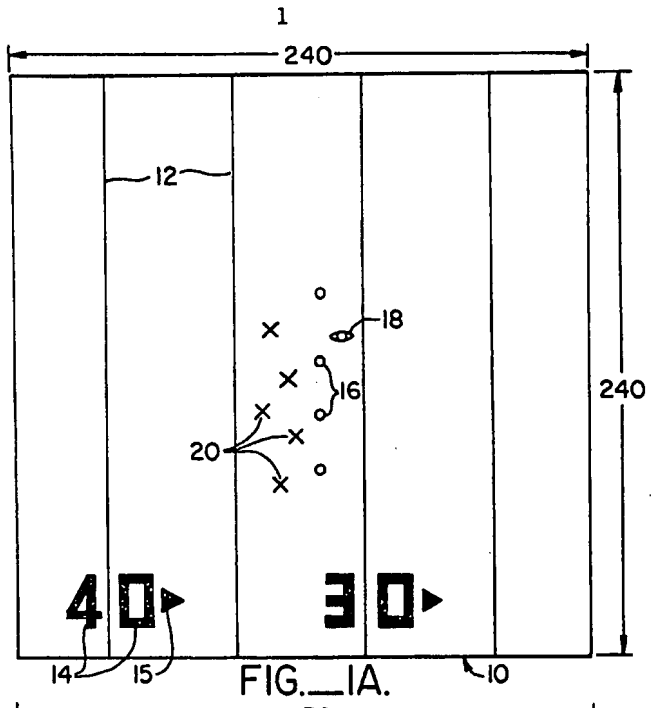

FIG._IA.

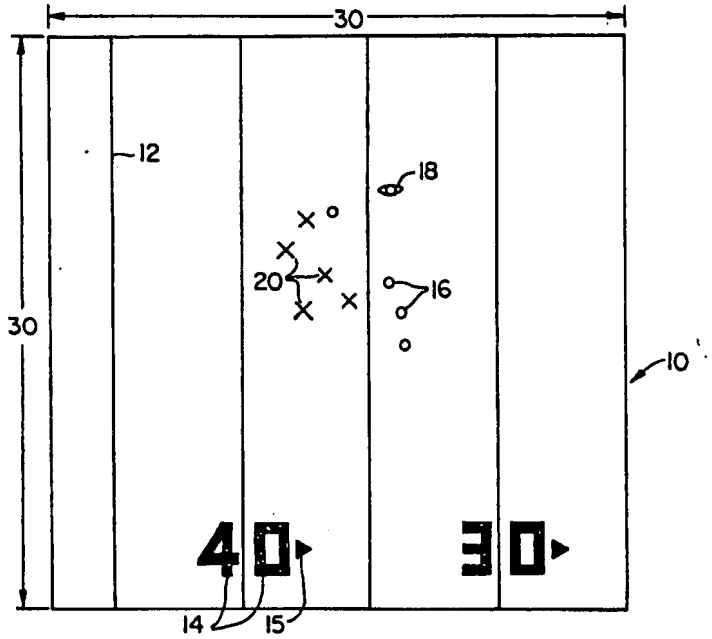

FIG._IB.

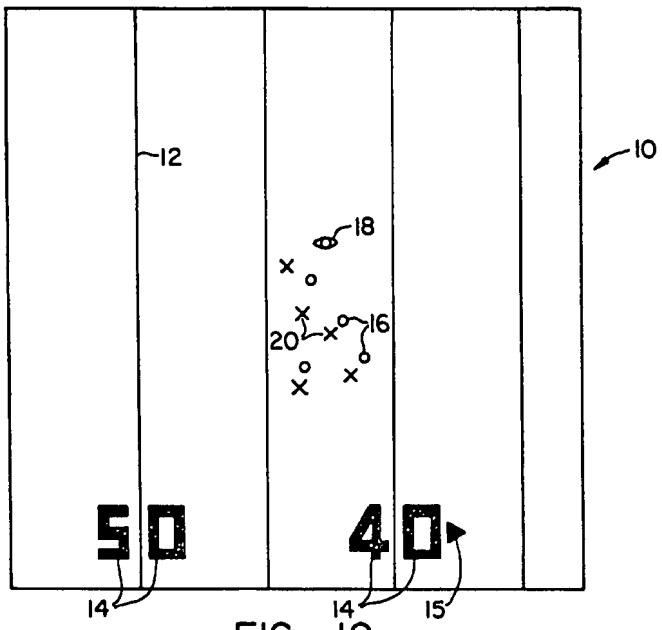

FIG._IC.

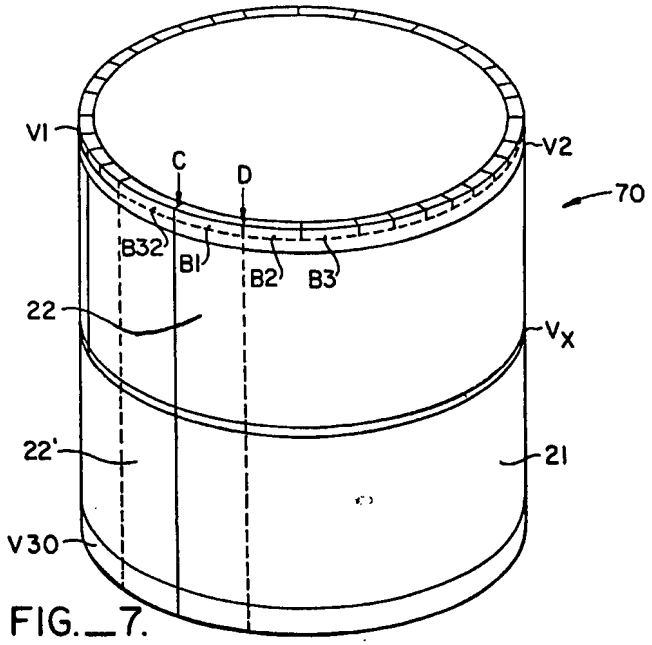

FIG._7.

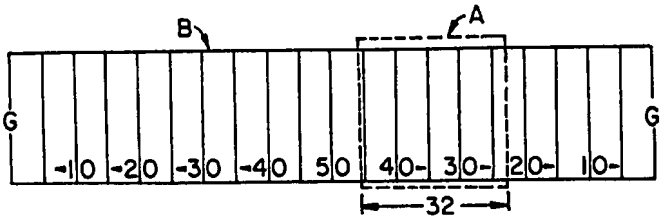

FIG._2.

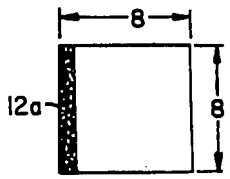

FIG._3A.

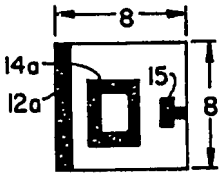

FIG._3B.

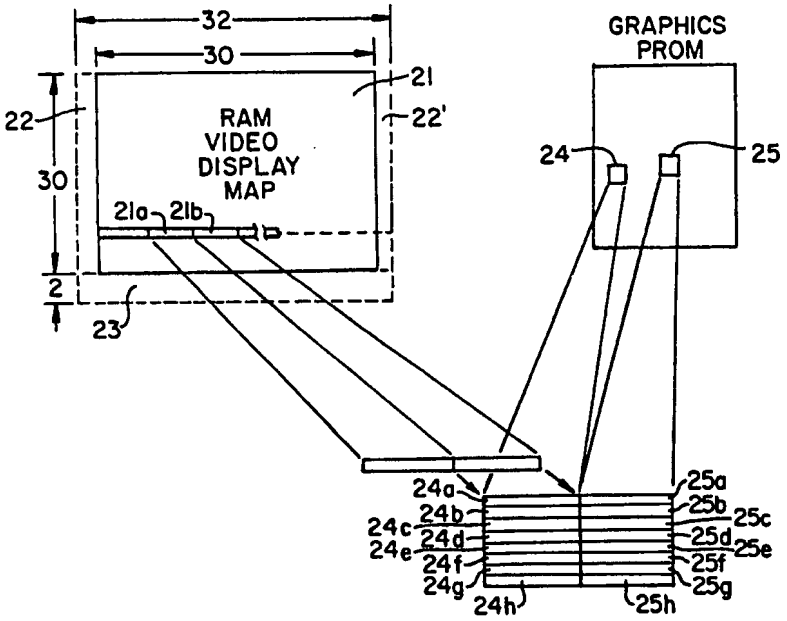

FIG._4.

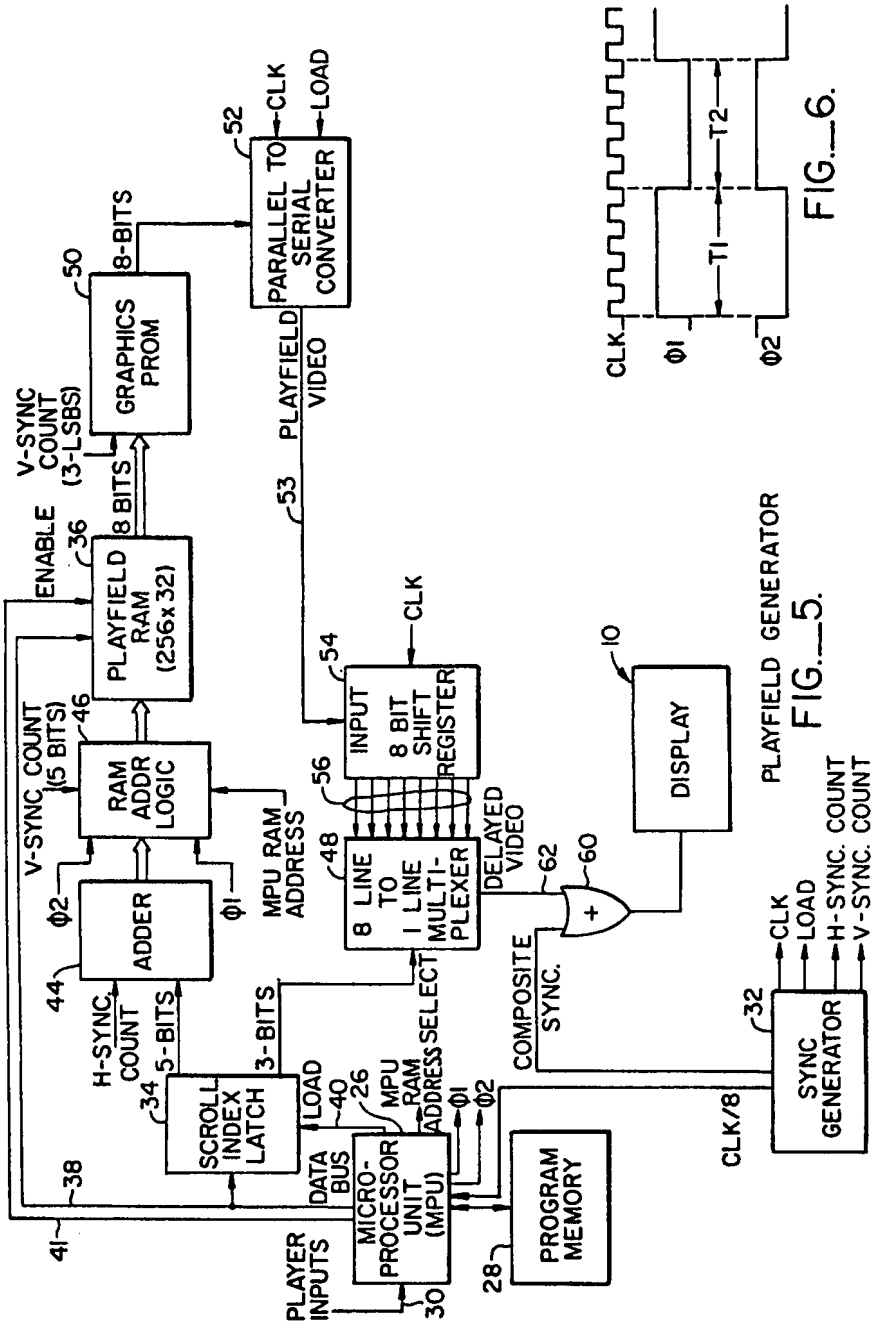

FIG. 6.

PLAYFIELD GENERATOR

FIG. 5.

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11th January 1980

Sir

European Patent Application No.80300076.9
in the name of Atari, Inc.
Our Case: J.14462 Europe

It has been noted that there is a clerical error on page 9, line 34 of the specification of the above application. As is quite evident from the context of the sentence in question, the number "10" should be replaced by the number "2^{10}". We should be grateful if you would effect such an amendment in the specification on file.

Yours faithfully

K.D.L. Beresford
Authorised Representative

The correction is allowed
The Hague, 30.05.80
Receiving Section

7/16/2007, EAST Version: 2.1.0.14

European Patent Office

EUROPEAN SEARCH REPORT

Application number
EP 80 30 0076

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
	US - A - 4 129 859 (M. IWAMURA et al.) * Figures 1,2,4,5; column 2, line 52 - column 3, line 4; column 3, lines 10-42; column 4, line 13 - column 5, line 9 * --	1,4,5, 7-9, 12	G 09 G 1/16 A 63 F 9/22
	US - A - 3 611 348 (W.P. ROGERS) * Figure 1; column 3, line 1 - column 4, line 18 * --	1-3, 10,12	TECHNICAL FIELDS SEARCHED (Int.Cl. ³)
	US - A - 4 068 225 (E.P. LEE) * Figure 4; column 5, lines 7-20 * ----	1	G 09 G 1/16 A 63 F 9/22

CATEGORY OF CITED DOCUMENTS

- X: particularly relevant
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- P: intermediate document
- T: theory or principle underlying the invention
- E: conflicting application
- D: document cited in the application
- L: citation for other reasons

&: member of the same patent family, corresponding document

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	29-04-1980	VAN ROOST

EPO Form 1503.1 06.78